IN THE CLAIMS:

Please amend the claims as follows. The claims are in the format as required by 35 C.F.R. § 1.121.

1. **(Currently Amended)** A method for tracking a ~~CDMA~~ pilot channel signal to discipline an oscillator, comprising:

downconverting an RF signal from a RF center frequency f_{RF} to an intermediate center frequency f_L where f_L is greater than or equal to a ~~CDMA~~ chip rate f_c, wherein downconverting includes incorporating bandpass filtering to remove extraneous signals while passing said ~~CDMA~~ pilot channel signal;

converting a signal format from analog to digital using a single analog-to-digital converter employing a sampling rate of f_s to create a digital signal $\{s(n)\}$;

employing a correlation circuit to establish a correlation between $\{s(n)\}$ and locally generated versions of I-channel and Q-channel PN signals, $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$, respectively; and

generating an estimate of a frequency error of the oscillator using correlation values corresponding to (2M+1) time shifts of $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$, the (2M+1) time shifts being $K-\Delta_M$, $K-\Delta_{(M-1)}, \ldots, K-\Delta_2, K-\Delta_1$, K, and $K+\Delta_1, K+\Delta_2, \ldots, K+\Delta_{(M-1)}, K+\Delta_M$, where a time shift of K corresponds to a time shift that provides <u>a</u> ~~the~~ maximum correlation value, and M is greater than or equal to 1,

<u>wherein correlation values are averaged over multiple periods of the PN signals.</u>

2. **(Original)** The method of claim 1, wherein the sampling rate, f_s, the intermediate center frequency, f_L, and the chip rate f_c are related by $f_s=4f_c$, and $f_L=f_c+kf_s$ for k=0.

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Attorney Docket No.
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3. **(Original)** The method of claim 1, wherein the sampling rate, f_s, the intermediate center frequency, f_L, and the chip rate f_c, are related by $f_s = 4f_c$, and $f_L = f_c + kf_s$ for k=1.

4. **(Original)** The method of claim 1, wherein the sampling rate, f_s, the intermediate center frequency, f_L, and the chip rate f_c, are related by $f_s = 4f_c$, and $f_L = f_c + kf_s$ for k=2.

5. **(Original)** The method of any of claims 2-4, wherein the correlation circuit uses a single accumulator for generating both an in-phase ("real") part and a quadrature ("imaginary") part of a complex correlation between the digital signal $\{s(n)\}$ and a given time shifted version of the locally generated versions of $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$.

6. **(Original)** The method of claim 5, wherein both positive overflows and negative underflows are monitored.

7. **(Original)** The method of claim 1, wherein a matched filter is not employed.

8. **(Original)** A receiver for performing the method of claim 1.

9. **(Original)** The method of claim 1, wherein the correlations are computed at time shift lags which are commensurate with the sampling rate.

10. **(Currently Amended)** The method of claim 9, wherein the correlations for lags smaller than the sampling interval are synthesized using a digital signal processing.

11. **(Original)** A receiver for performing the method of claim 1, further comprising an autonomous background correlator.

12. **(Original)** A receiver for performing the method of claim 1, further comprising an autonomous background correlator computing correlations over a period less than the time period of the PN signals.

13. **(Cancel)**

14. **(Currently Amended)** An apparatus to track a pilot signal, comprising:

a correlator circuit adapted to compute a complex correlation between a received version of the pilot signal and locally generated versions of I-channel and Q-channel PN signals, $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$, respectively; and

a signal processor circuit coupled to the correlator circuit,

wherein the signal processor circuit averages correlation values over multiple periods of the PN signals.

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15. **(Original)** The apparatus of claim 14, wherein said correlator circuit includes an FPGA.

16. **(Original)** The apparatus of claim 14, wherein the correlator circuit includes a single accumulator that computes both the real and imaginary part of the complex correlation.

17. **(Cancel)**

18. **(Currently Amended)** The apparatus of claim 14, wherein said signal processor circuit includes a DSP.

19. **(Cancel)**

20. **(Currently Amended)** A receiver including two of the apparatus according to claim 14 that are operated in parallel to track multiple pilots.

21. **(Original)** The receiver of claim 20, wherein at least one correlator computes correlation values over a time period of less than one period of the PN signals and is used as an autonomous background correlator.

22. **(Original)** A method of tracking a CDMA pilot signal that comprises utilizing the apparatus of claim 14.

23. **(Currently Amended)** A method for tracking a ~~CDMA~~ pilot channel to discipline an oscillator, comprising:

downconverting the RF signal from the RF center frequency, f_{RF} to an intermediate center frequency of f_L, where f_L is greater than or equal to the ~~CDMA~~ chip rate, f_c, said

downconversion incorporating bandpass filtering to remove extraneous signals while passing said pilot channel signal;

converting signal format from analog to digital using a single analog-to-digital converter employing a sampling rate of f_s, to create the digital signal $\{s(n)\}$;

employing correlation to establish the correlation between $\{s(n)\}$ and locally generated versions of the I-channel and Q-channel PN signals, $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$, respectively; and generating an estimate of the frequency error of the oscillator using correlation values corresponding to (2M+1) time shifts of the locally generated versions of $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$, said time shifts being $K-\Delta_M$, $K-\Delta_{(M-1)}$, . . . , $K-\Delta_2$, $K-\Delta_1$, K, and $K+\Delta_1$, $K+\Delta_2$, . . . , $K+\Delta_{(M-1)}$, $K+\Delta_M$, where time shift of K corresponds to the time shift that provides the maximum correlation value, and the value of M is 4,

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wherein correlation values are averaged over multiple periods of the PN signals.

24. **(Currently Amended)** A method of tracking a pilot channel, comprising:

disciplining an oscillator including generating a spectrum shaped channel pilot signal $\{\gamma(n)\}$ from a chip-rate PN sequence $\{i(n)\}$ by:

oversampling the chip-rate PN sequence $\{i(n)\}$ at a higher sampling rate to yield a signal $\{a(n)\}$;

passing $\{a(n)\}$ through a first FIR filter whose impulse response coefficients are $\{g(n)\}$ to yield a signal $\{\beta(n\}$; and

filtering $\{\beta(n\}$ with a second FIR filter to yield the spectrum shaped channel pilot signal $\{\gamma(n)\}$; and

averaging correlation values over multiple periods of the chip-rate PN signal.

25. **(Original)** The method of claim 24, wherein the spectrum shaped channel pilot signal $\{\gamma(n)\}$ is a spectrum shaped I-channel pilot signal.

26. **(Original)** The method of claim 24, wherein both positive overflows and negative overflows are monitored.

27. **(Original)** The method of claim 24, further comprising translating the spectrum shaped I channel pilot signal {$\gamma(n)$} down to a zero-offset-carrier frequency signal {$s(n)$}.

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28. **(Original)** The method of claim 27, further comprising translating the zero-offset-carrier frequency signal {$s(n)$} down to a baseband signal {$w(n)$}.

29. **(Original)** The method of claim 24, wherein a sampling clock is derived from a VCXO that is phase-locked to a reference frequency.

30. **(Original)** The method of claim 24, wherein a correlation is computed at lags which are commensurate with a sampling rate.

31. **(Original)** The method of claim 24, wherein a matched filter is not employed.

32. **(Original)** A receiver for performing the method of claim 24.

33. **(Previously Presented)** The method of claim 24, wherein the spectrum shaped channel pilot signal {$\gamma(n)$} is a spectrum shaped Q-channel pilot signal.

34. **(Currently Amended)** An apparatus to track a pilot signal, comprising:

a correlator circuit adapted to oversample a chip-rate PN sequence {$I(n)$} at a higher sampling rate to yield a signal {$a(n)$}, pass {$a(n)$} through a first FIR filter whose impulse response coefficients are {$g(n)$} to yield a signal {$\beta(n$}; and filter {$\beta(n$} with a second FIR filter to yield a spectrum shaped pilot channel signal {$\gamma(n)$}<u>; and</u>

<u>a signal processor circuit coupled to the correlator circuit,</u>

<u>wherein the signal processor circuit averages correlation values over multiple periods of the chip-rate PN sequence</u>.

35. **(Original)** The apparatus of claim 34, wherein said correlator circuit include a FPGA.

36. **(Cancel)**

37. **(Original)** The apparatus of claim 34, wherein said signal processor circuit includes a DSP.

38. **(Currently Amended)** The apparatus of claim ~~36~~34, further comprising an A/D converter coupled to said signal processor circuit.

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39. **(Previously Presented)** The apparatus of claim 34, wherein the first FIR filter includes a 4-point FIR filter having all 4 coefficients at least substantially equal.

40. **(Previously Presented)** The apparatus of claim 34, wherein the second FIR filter includes a 48-point FIR filter.

41. **(Previously Presented)** A method of tracking a CDMA pilot channel which comprises utilizing the apparatus of claim 34.

42. **(Previously Presented)** The apparatus of claim 34, further comprising an autonomous background correlator coupled to the correlator circuit.

43. **(Currently Amended)** A receiver comprising at least two of the apparatus according to claim 34 that are operated in parallel to track multiple pilots.

44. **(New)** The method of claim 1, wherein averaging includes averaging C_{MS} over multiple correlation computations to reduce noise

45. **(New)** The apparatus of claim 14, wherein the signal processor averages C_{MS} over multiple correlation computations to reduce noise.

46. **(New)** The method of claim 24, wherein averaging includes averaging C_{MS} over multiple correlation computations to reduce noise.

47. **(New)** The apparatus of claim 34, wherein the signal processor averages C_{MS} over multiple correlation computations to reduce noise.

48. **(New)** The method of claim 10, wherein using digital signal processing includes synthesizing an offset to improve precision of an estimate of time-of-arrival of a received pilot

code.

49. (New) The apparatus of claim 18, wherein the DSP synthesizes an offset to improve precision of an estimate of time-of-arrival of a received pilot code.

50. (New) The method of claim 24, wherein the correlations for lags smaller than the sampling interval are synthesized using digital signal processing.

51. (New) The method of claim 50, wherein using digital signal processing includes synthesizing an offset to improve precision of an estimate of time-of-arrival of a received pilot code.

52. (New) The apparatus of claim 34, wherein the DSP synthesizes an offset to improve precision of an estimate of time-of-arrival of a received pilot code.

53. (New) The method of claim 1, further comprising employing another correlator circuit in parallel to track multiple pilots.

54. (New) The method of claim 24, further comprising disciplining another oscillator in parallel to track multiple pilots including generating another spectrum shaped channel pilot signal by:

oversampling to yield another signal;

passing the another signal through another FIR filter; and

filtering with another second FIR filter to yield the another spectrum shaped channel pilot signal.

55. (New) The method of claim 1, wherein the correlation circuit is time shared to track multiple pilots.

56. (New) The apparatus of claim 14, wherein the correlator circuit is time shared to track multiple pilots.

57. (New) The method of claim 24, further comprising time sharing a correlator circuit to

track multiple pilots.

58. (New) The apparatus of claim 34, wherein the correlator circuit is time shared to track multiple pilots.

59. (New) The method of claim 1, wherein the I-channel and Q-channel PN signals are different.

60. (New) The apparatus of claim 14, wherein the I-channel and Q-channel PN signals are different.

61. (New) The method of claim 24, wherein disciplining an oscillator includes generating another spectrum shaped channel pilot signal from another different chip-rate PN sequence.

62. (New) The apparatus of claim 34, wherein the correlator circuit adapted to oversample another different chip-rate PN sequence.